PLL bringup:
1. VCTCXO starts up
2. FX3 brings up transceiver, sets CLKOUT to FPGA
3. FX3 programs FPGA
4. FPGA writes to PLL, initializes PLL
5. PLL locks to external ref if avail.
6. If no ref, PLL tristated via SPI

SMA External Reference

15dBm max. (3.5V into 50 ohms)

J100 142-0701-871
C100 0.1uF
R128 10K
D100
R126 10K
C104 0.1uF
R110 49.9
3.3V_CLK:1

C111 0.1uF

DG4157DL U103
SN74LVC1G3157 works too
ref_sel

C150 0.1uF

C106 0.1uF
C107 0.1uF
C112 100pF
C151 0.1uF
xo_to_pll

ADF4001 U101
CE, RFIN_A, RFIN_B, REFIN, Rset
AVDD, AVDD, DVDD, DVDD, VP
AGND, AGND, DGND, DGND, PAD
CP, CPGND, MUXOUT, SCLK, SDA, SLE
pll_lock_filt, pll_sclk_filt, pll_mosi_filt, pll_ce_filt

R111 4.7K

C137 180pF
R124 100K
R125 47.0K 1%
C138 2.2nF
C139 82pF
R120 1M
R121 1M
R118 DNP
auxdac1
vcxo_tune

Assume 400Hz/Volt
4kHz loop bandwidth
10MHz compare frequency
5mA CP current
reduce C139 by the load cap of trace + tune
Eff. Kv is adjusted based on the resistor div
formed by R124 and the impedance
of Cat DAC when disabled (if R118 installed)

CONFIGURE PLL_LOCK AS OPEN DRAIN!

LAYOUT:
R110 and C150 Should be close to U101

GPSDO

L100 MI1206K601R-10
C101 0.1uF
C102 22uF X5R 6.3V

U100 M9107
R100 4.7K
J101 142-0701-871
PPS_In, Antenna, Enter_ISP, Serial_In
gps_rxd
10MHz_Out, Lock_OK, PPS_Out, 5V_Out, NMEA_Out, Serial_Out
gps_lock, PPS_IN_INT, gps_txd_nmea, gps_txd
GND, GND, GND, GND
R106 100
R127 150
C108 47uF 6.3V X5R

GPS antenna

S100 JLEAD_SW

R108 150
LED100 GPSDO lock LED
Q100
gps_lock
R109 10K

L107 MI1206K601R-10
C105 10uF X5R 6.3V
C109 0.1uF
VCTCXO X100
vcxo_tune
C119 470pF

R122 510K
R123 510K
C118 0.01uF

C115 470pF
C120 470pF
C121 470pF
C122 470pF

pll_lock R101 2.2K pll_lock_filt
pll_sclk R105 1K pll_sclk_filt
pll_mosi R107 1K pll_mosi_filt
pll_ce R112 1K pll_ce_filt

C117 0.1uF
Place at U106

U106 SN74LVC1G04
net=3.3V_CLK:5
net=GND:3
Self-biasing clock squarer

U104 CDLVC1103PWR
CLKIN, 1G
Y0, Y1/NC, Y2/NC, Y3/NC
R113 47 xo_out To transceiver
R119 47 xo_to_pll To PLL RF in

U105 FIN1001
codec_main_clk_p
codec_main_clk_n
Buffer to FPGA
Place near U104
net=3.3V_CLK:1
net=GND:2

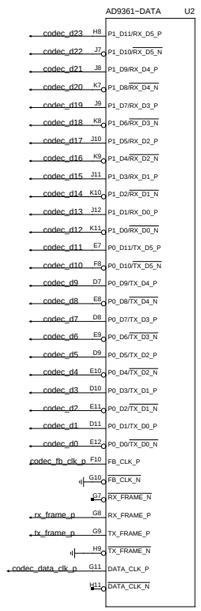
C110 10uF X5R 6.3V
C113 0.1uF
C114 0.1uF
Place at U105

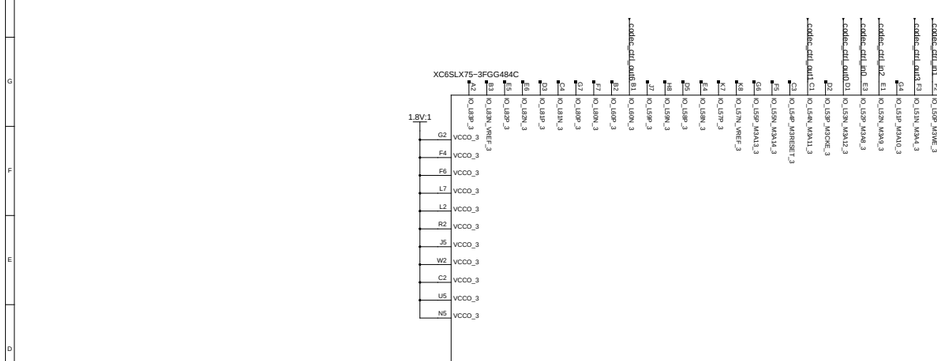
External PPS input

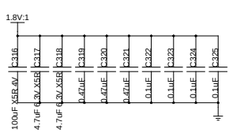
5V max.

J104 142-0701-971
R103 1K
R102 49.9
C103 1000pF
R104 2K
U102 SN74AUP1T57
A, B, C, Y, Vcc, GND
PPS_IN_EXT
C116 0.1uF

TITLE	B200 Clock
FILE: clock.sch	REVISION: 2
PAGE 1 OF 8	DRAWN BY: nick, matt

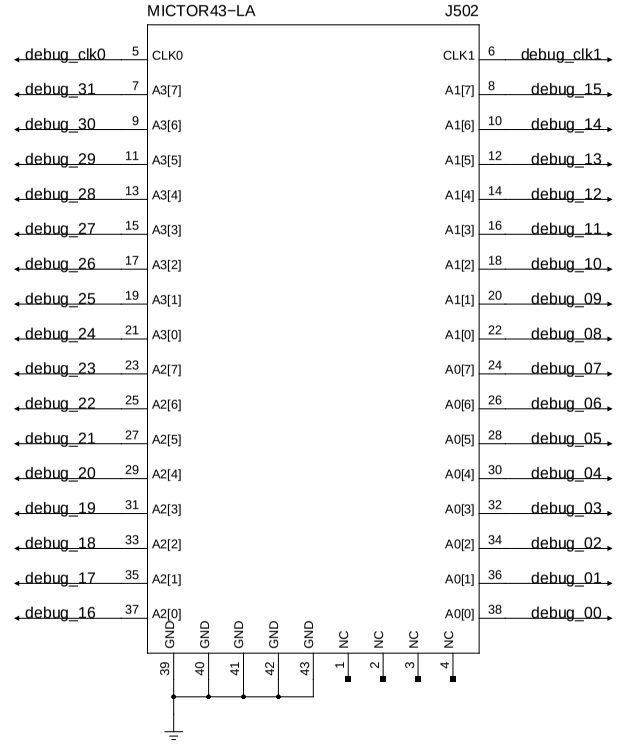


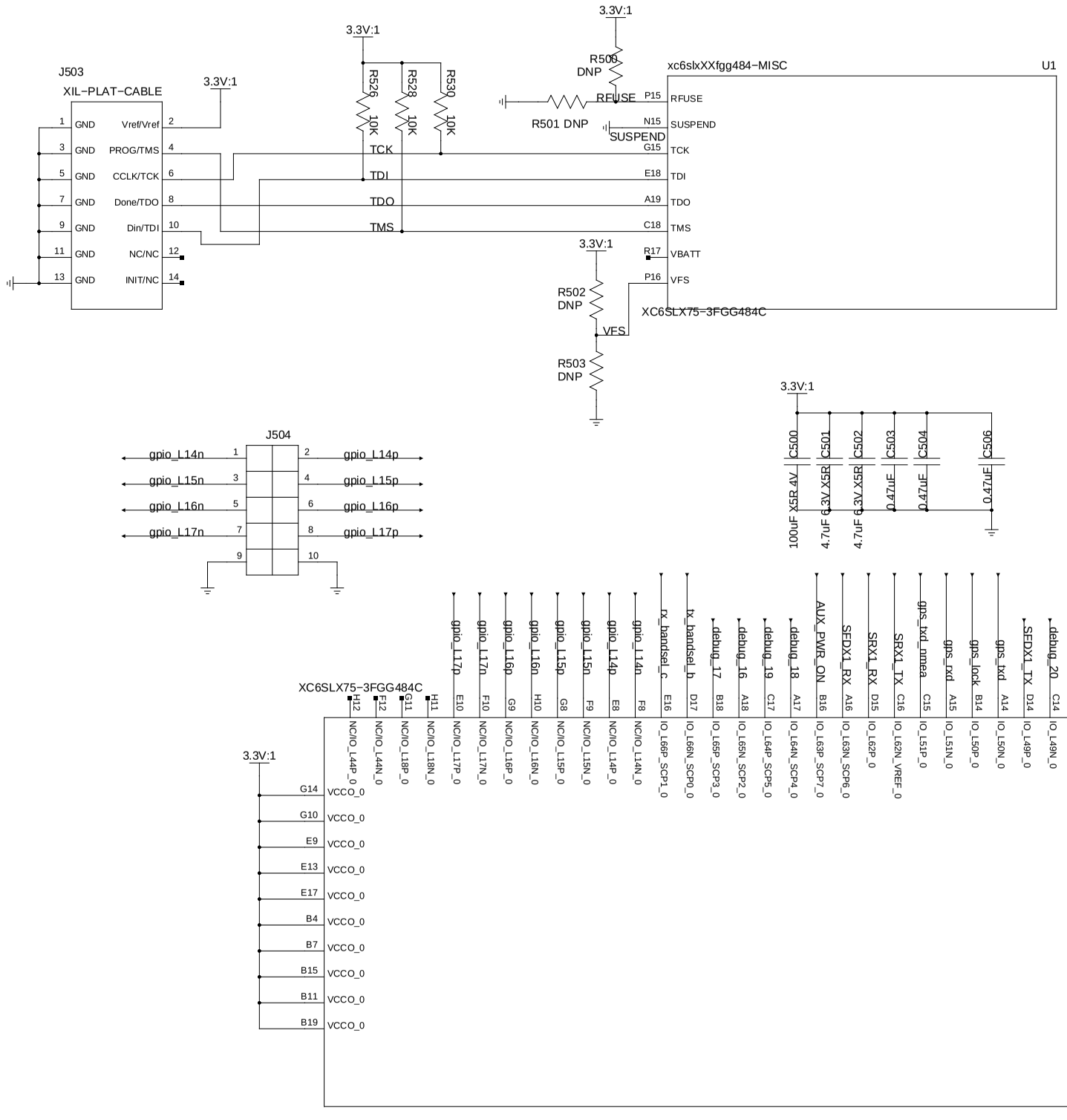


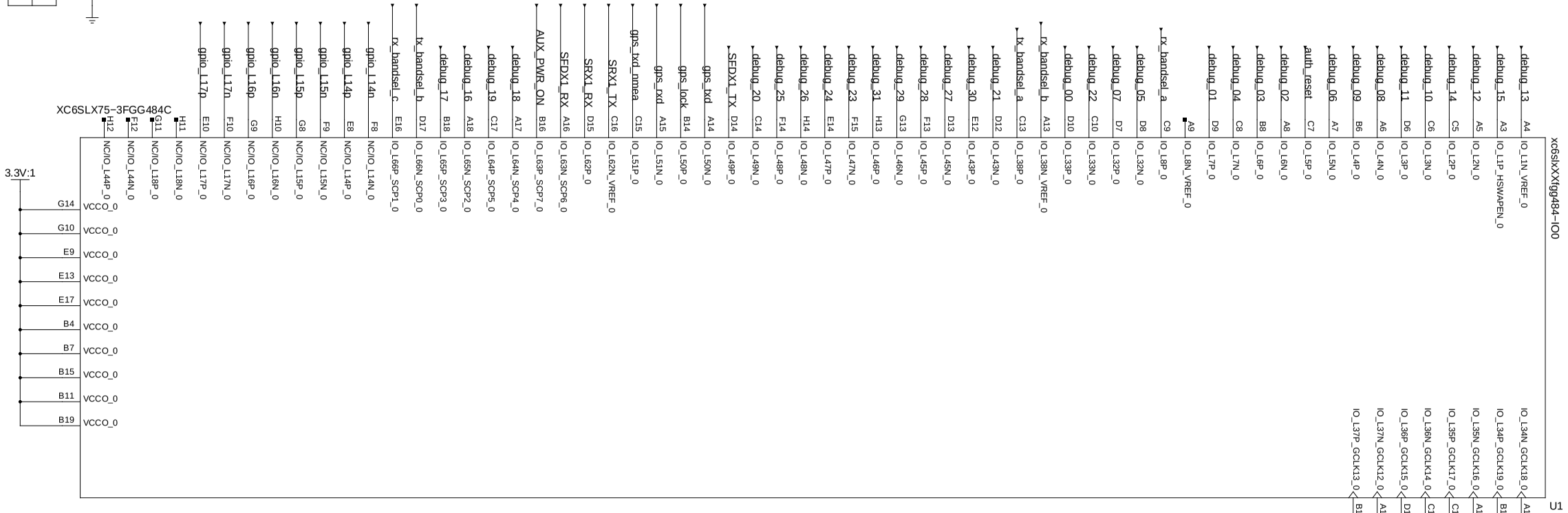


TITLE	B200 AD9361-FPGA Interface
FILE: fpga_codec.sch	REVISION: 2
PAGE 2 OF 8	DRAWN BY: nick, matt

debug connector

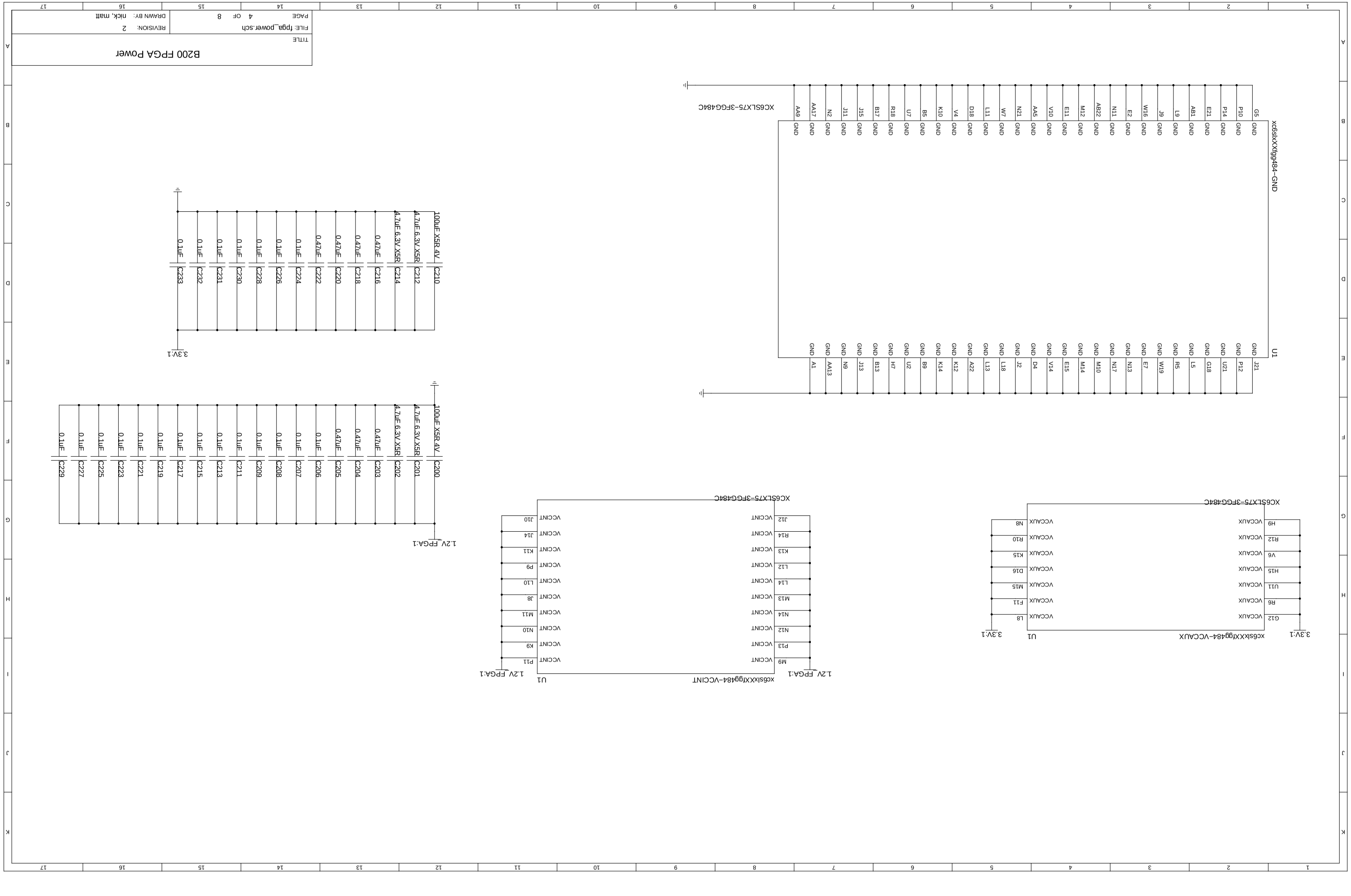


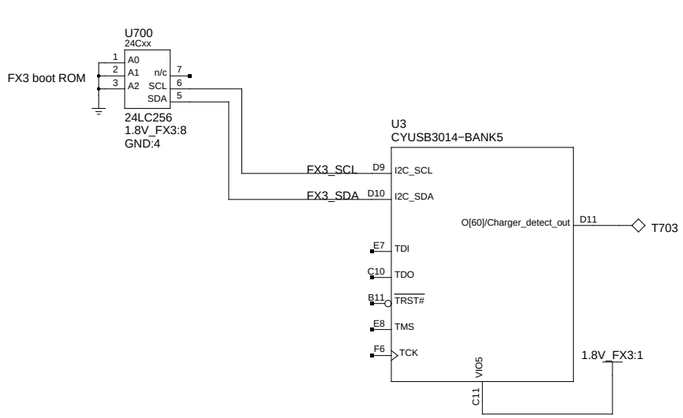


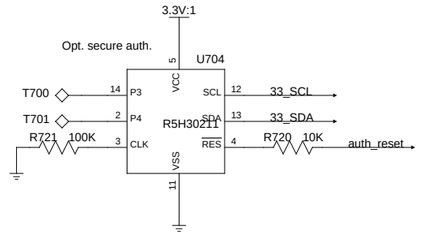


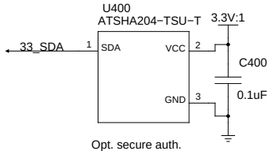
B200 debug and misc

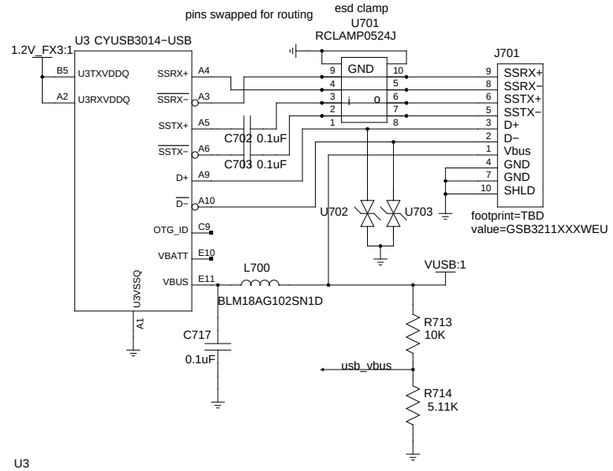
TITLE			
FILE: fpga_debug.sch		REVISION: 2	
PAGE 3 OF 8		DRAWN BY: nick, matt	

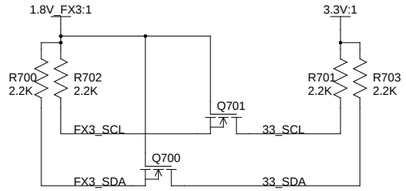

B200 FPGA Power
TITLE
FILE: fpga_power.sch
REVISION: 2
DRAWN BY: nick, matt
PAGE 4 OF 8
xc6slxXfgg484-GND
U1
XC6SLX75-3FGG484C
GND
xc6slxXfgg484-VCCINT
VCCINT
1.2V_FPGA:1
xc6slxXfgg484-VCCAUX
VCCAUX
3.3V:1
100uF X5R 4V
4.7uF 6.3V X5R
0.47uF
0.1uF

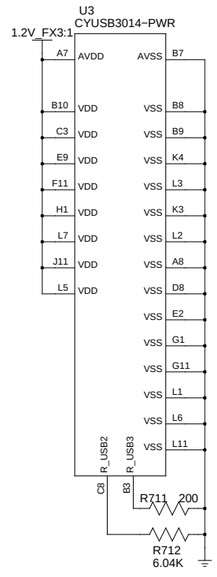


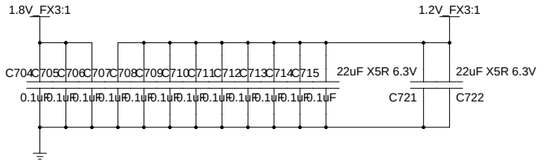




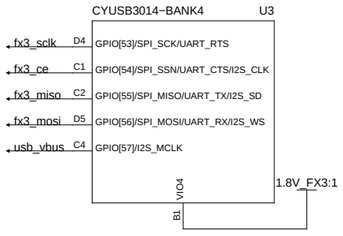


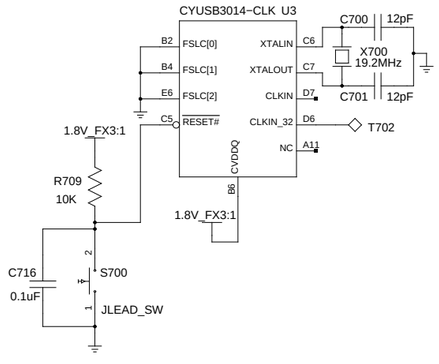






SPI is unusable in 32−bit GPIF mode.



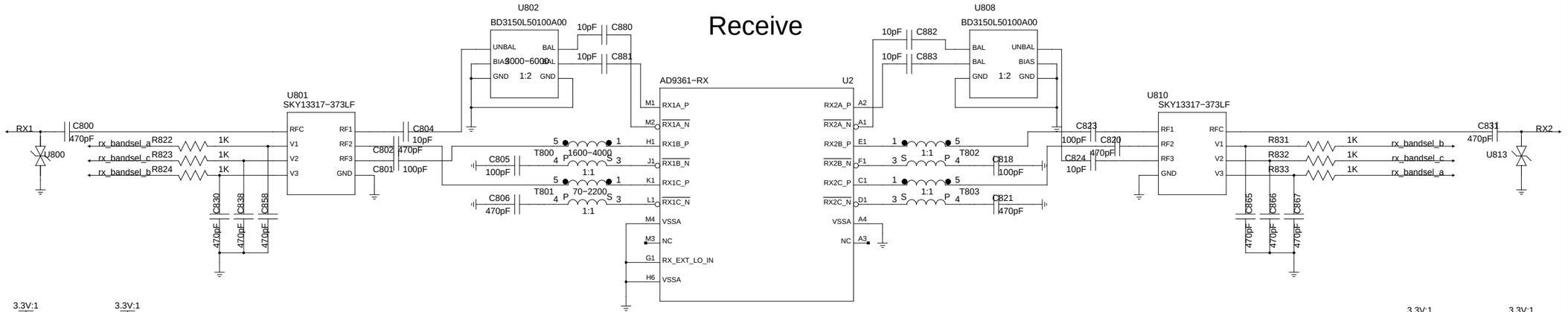


TITLE	B200 FX3 interface
FILE: fx3.sch	REVISION: 2
PAGE 5 OF 8	DRAWN BY: nick, matt

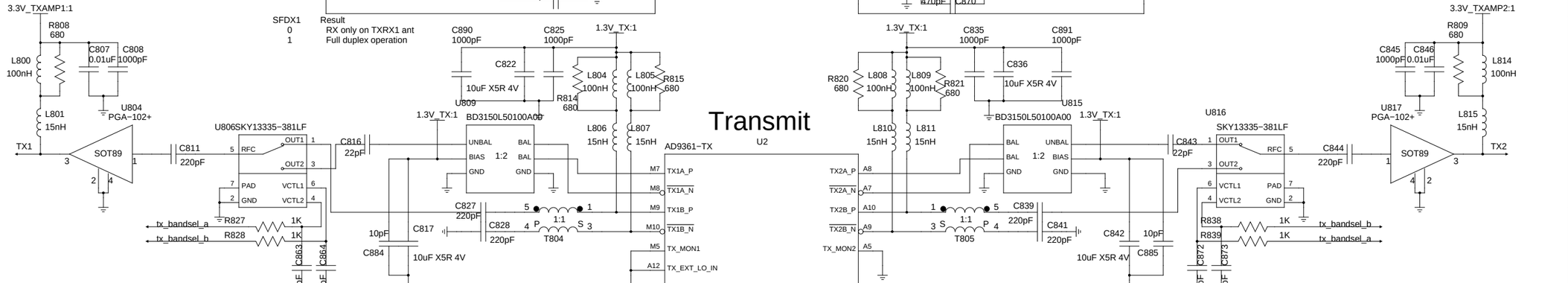
B200 FX3 GPIF interface

FILE: gpif.sch
DRAWN BY: nick.mattt
REVISION: 2
PAGE 6 OF 8

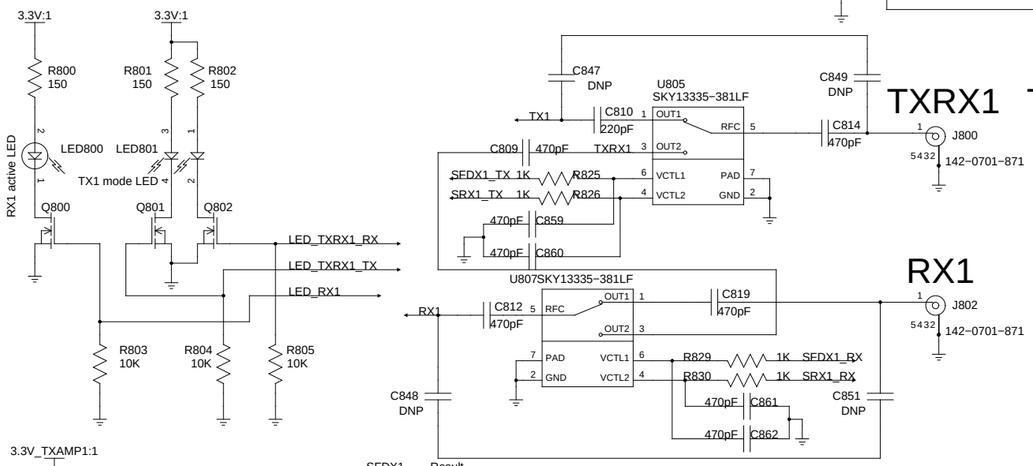
Receive



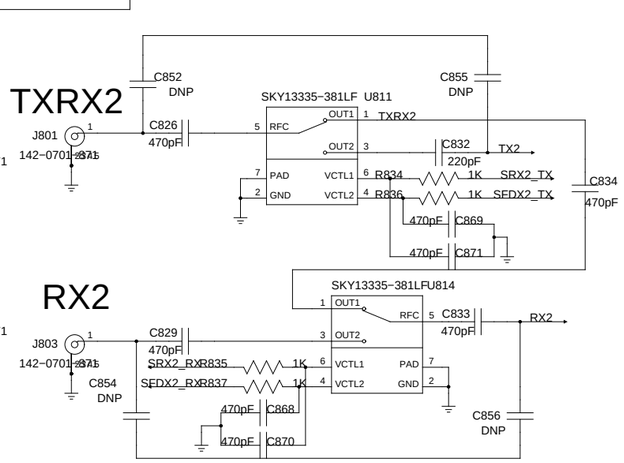
Transmit

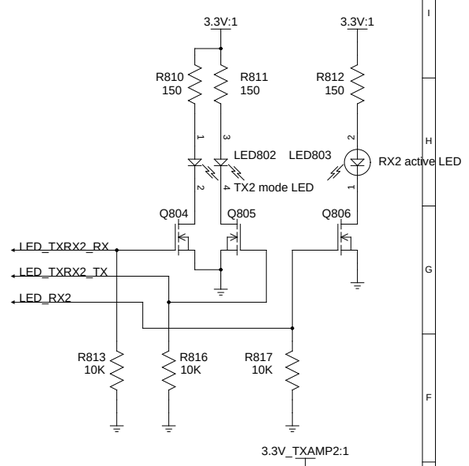


TXRX1



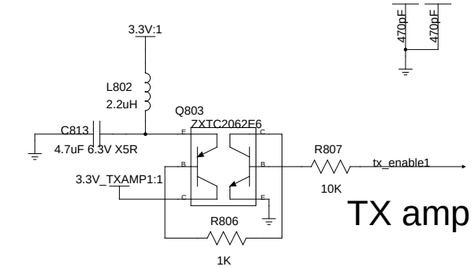
TXRX2

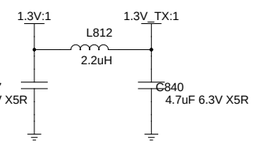


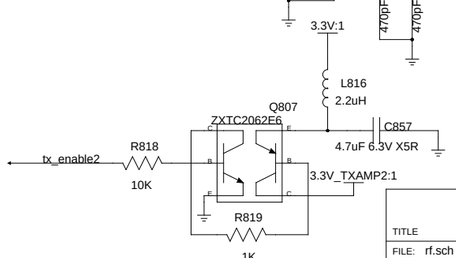


SFDX1	Result
0	RX only on TXRX1 ant
1	Full duplex operation

TX amp power





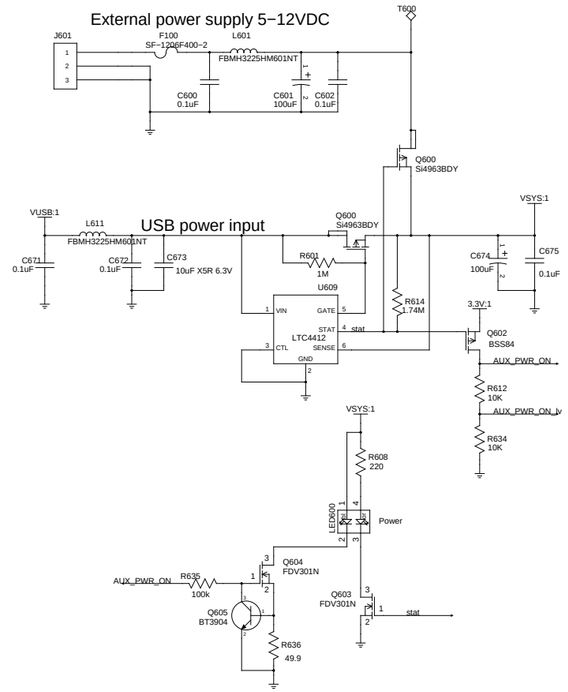


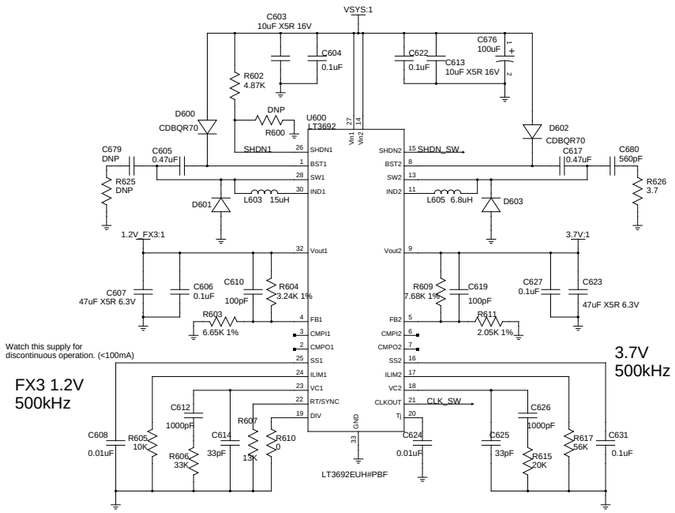
B200 RF Interface

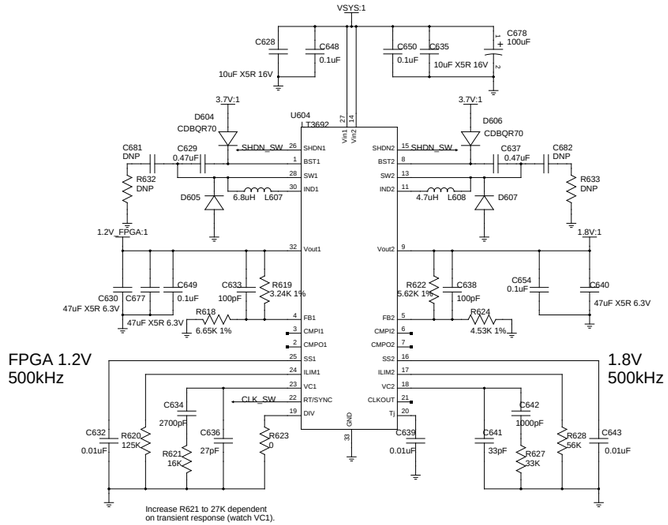
TITLE

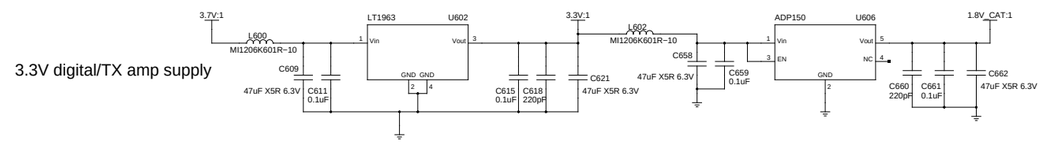
FILE: rf.sch | REVISION: 2

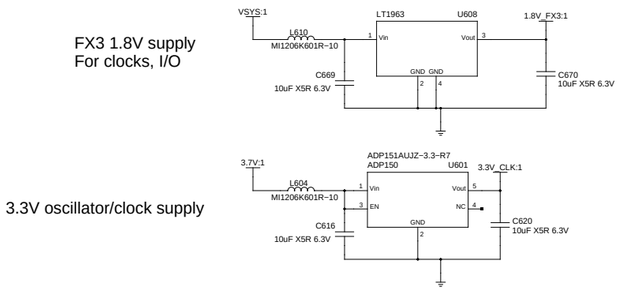
PAGE 8 OF 8 | DRAWN BY: nick, matt

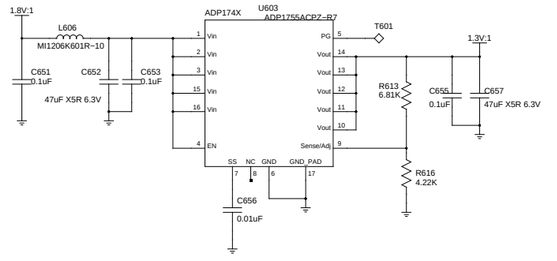


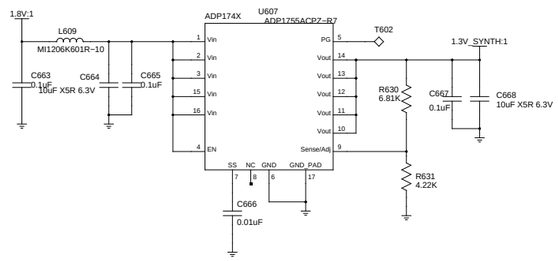


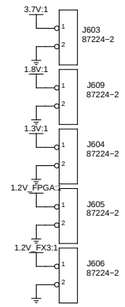












TITLE	B200 Power
FILE: power.sch	REVISION: 2
PAGE 7 OF 8	DRAWN BY: nick, matt