MC14495-1

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HEXADECIMAL-TO-SEVEN SEGMENT LATCH/DECODER LED DRIVER

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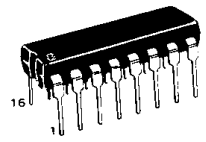
HEXADECIMAL-TO-SEVEN SEGMENT LATCH/ DECODER LED DRIVER

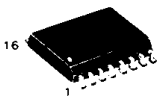
The MC14495-1 is constructed with CMOS enhancement-mode devices and NPN bipolar output drivers in a monolithic structure. The circuit provides the functions of a 4-bit storage latch. The decoder is implemented utilizing a mask-programmable ROM. With a 5-volt power supply, it can be used without resistor interface to drive seven segment LEDs. The series output resistors of, typically, 290 ohms are internal to the device.

Applicatons include MPU systems display driver, instrument display driver, computer/calculator display driver, clockpit display driver, and various clock, watch, and timer uses.

- Low Logic-Circuit Power Dissipation
- High Current-Sourcing Outputs with Internal Limiting Resistors
- Latch Storage of Code
- Supply Voltage Range = 4.5 to 18 V
- CMOS Input Switching Levels
- Standard ROM Provides Hex-to-Seven Segment Decoding
- Other ROM Options Available Upon Request (Contact your Motorola Sales Office)
- Chip Complexity: 187 FETs plus 9 NPNs or 49 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

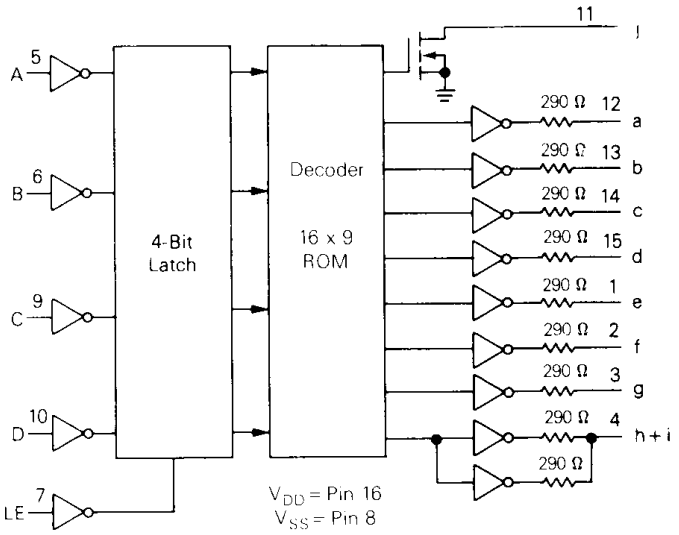


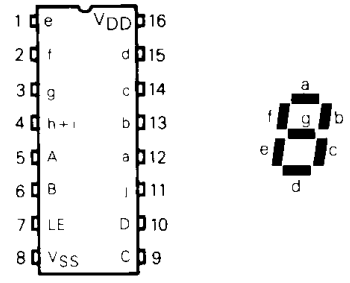
DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

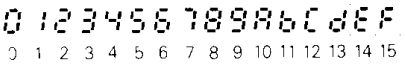
MC14495P1	Plastic DIP
MC14495DW1	SOG Package

BLOCK DIAGRAM





ALPHANUMERIC DISPLAY



TRUTH TABLE (LE = Low)

INPUTS				OUTPUTS								
D	C	B	A	a	b	c	d	e	f	g	h+i	DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	Open 0
0	0	0	1	0	1	1	0	0	0	0	0	Open 1
0	0	1	0	1	1	0	1	1	0	1	0	Open 2
0	0	1	1	1	1	1	1	0	0	1	0	Open 3
0	1	0	0	0	1	1	0	0	1	1	0	Open 4
0	1	0	1	1	0	1	1	0	1	1	0	Open 5
0	1	1	0	1	0	1	1	1	1	1	0	Open 6
0	1	1	1	1	1	1	0	0	0	0	0	Open 7
1	0	0	0	1	1	1	1	1	1	1	0	Open 8
1	0	0	1	1	1	1	1	0	1	1	0	Open 9
1	0	1	0	1	1	1	0	1	1	1	1	Open A
1	0	1	1	0	0	1	1	1	1	1	1	Open b
1	1	0	0	1	0	0	1	1	1	0	1	Open C
1	1	0	1	0	1	1	1	1	0	1	1	Open d
1	1	1	0	1	0	0	1	1	1	1	1	Open E
1	1	1	1	1	0	0	0	1	1	1	1	0 F

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25°C Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	P_{OHmax}‡	 50 100	mW

‡ $P_{OHmax} = I_{OH}(V_{DD}-V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

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ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ#	25°C Max	85°C Min	85°C Max	Unit
Input Voltage "0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)		5	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)		15	–	4.0	–	6.00	4.0	–	4.0	
(V_O = 0.5 or 3.8 V) "1" Level	V_{IH}	5	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage: a−g, h+i	V_{OL}	5	–	0.1	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0, $I_{out} = 0\ \mu A$		10	–	0.1	–	0	0.05	–	0.05	
		15	–	0.1	–	0	0.05	–	0.05	
Output Drive Voltage: a−g, h+i	V_{OH}	5								V
(I_{OH} = 0 mA)			4.0	–	4.0	4.8	–	4.0	–	
(I_{OH} = 5 mA)			2.45	–	2.4	3.0	–	2.05	–	
(I_{OH} = 10 mA)			1.3	–	0.8	1.7	–	–	–	
(I_{OH} = 0 mA)		10	9.0	–	9.0	9.8	–	9.0	–	V
(I_{OH} = 5 mA)			7.4	–	7.2	8.0	–	6.9	–	
(I_{OH} = 10 mA)			6.4	–	5.8	6.7	–	5.0	–	
(I_{OH} = 15 mA)			5.3	–	4.4	5.3	–	3.05	–	
(I_{OH} = 0 mA)		15	14.0	–	14.0	14.8	–	14.0	–	V
(I_{OH} = 5 mA)			12.2	–	12.0	13.0	–	11.7	–	
(I_{OH} = 10 mA)			10.9	–	10.4	11.7	–	9.6	–	
(I_{OH} = 15 mA)			9.7	–	8.8	10.3	–	7.45	–	
(I_{OH} = 20 mA)			8.5	–	7.2	8.8	–	5.25	–	
(I_{OH} = 25 mA)			7.4	–	5.6	7.1	–	3.0	–	
Output Sink Current: j	I_{OL}									mA
(V_{OL} = 0.4 V)		5	–	–	0.3	1.00	–	–	–	
(V_{OL} = 0.5 V)		10	–	–	–	–	–	–	–	
(V_{OL} = 1.5 V)		15	–	–	0.5	1.25	–	–	–	
Input Current (L Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (P Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	0.3	–	0.08	0.25	–	0.2	mA
V_{in} = 0 or V_{DD}, $I_{out} = 0\ \mu A$		10	–	1.5	–	0.40	1.25	–	1.0	
(Per Package)		15	–	3.0	–	0.85	2.50	–	2.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5	$I_T = (1.9\ \mu A/kHz)f + I_{DD}$							μA
		10	$I_T = (3.8\ \mu A/kHz)f + I_{DD}$							
		15	$I_T = (5.7\ \mu A/kHz)f + I_{DD}$							

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD}f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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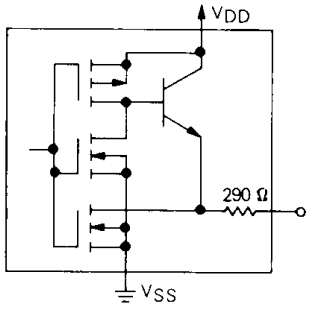
SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} V	Min	Typ#	Max	Unit
Output Rise Time, a–g, h+i Outputs (Figure 1)	t_{TLH}					ns
		5	–	210	450	
		10	–	145	300	
		15	–	90	200	
Output Fall Time, a–g, h+i Outputs (Figure 1)	t_{THL}					µs
		5	–	1.5	3.5	
		10	–	1.3	2.75	
		15	–	1.1	2.25	
Output Fall Time, j Output (Figures 3 and 4)	t_{THL}					ns
		5	–	105	250	
		10	–	40	100	
		15	–	30	75	
Propagation Delay Time, A, B, C, D to a–g, h+i Outputs (Figure 2)	t_{PLH}					ns
		5	–	935	2400	
		10	–	340	900	
		15	–	230	500	
	t_{PHL}	5	–	7.0	18.0	µs
		10	–	3.5	9.0	
		15	–	2.0	5.0	
Propagation Delay Time, A, B, C, D to j Output (Figures 3 and 4)	t_{PLZ}					µs
		5	–	11.0	25.0	
		10	–	8.0	20.0	
		15	–	4.0	10.0	
	t_{PZL}	5	–	800	1500	ns
		10	–	400	1000	
		15	–	200	500	
Propagation Delay Time, LE to a–g, h+i Outputs (Figure 5)	t_{PLH}					ns
		5	–	1300	3000	
		10	–	500	1500	
		15	–	350	1000	
	t_{PHL}	5	–	16.0	30.0	µs
		10	–	6.0	15.0	
		15	–	5.0	10.0	
Propagation Delay Time, LE to j Output (Figures 4 and 6)	t_{PLZ}					µs
		5	–	14.0	30	
		10	–	8.0	20	
		15	–	6.0	15	
	t_{PZL}	5	–	10.0	25	µs
		10	–	5.0	15	
		15	–	4.0	10	
Setup Time, A, B, C, D to LE (Figure 7)	t_{su}	5	100	35	–	ns
		10	65	25	–	
		15	65	25	–	
Hold Time, LE to A, B, C, D (Figure 7)	t_h	5	125	45	–	ns
		10	75	30	–	
		15	75	25	–	
Latch Enable Pulse Width, LE (Figure 7)	t_w	5	525	210	–	ns
		10	200	80	–	
		15	140	56	–	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OUTPUT CIRCUIT
(Except Pin 11)



INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h + i; PINS 12, 13, 14, 15, 1, 2, 3, 4)

The segment drivers are emitter-follower NPN transistors. To limit the output current, a resistor, typically 290 ohms, is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{DD} = 5.0$ volts.

OUTPUT (j; PIN 11)

This open-drain output is activated (goes low) whenever inputs A, B, C, and D are all set to a logic one. Otherwise the output is in the high-impedance state. See the truth table.

INPUT DATA (A, B, C, D; PINS 5, 6, 9, 10)

The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by the Latch Enable input.

LATCH ENABLE (LE; PIN 7)

The data on inputs A, B, C and D will pass through the latch and will be decoded immediately when LE is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when LE = low and will be latched with the rising edge of LE. The data will remain stored as long as LE is high.

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SWITCHING WAVEFORMS

Figure 1

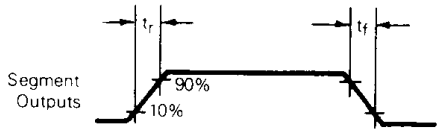


Figure 2

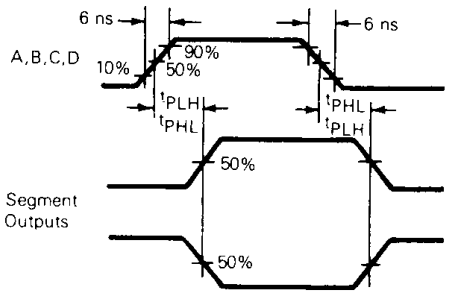


Figure 3

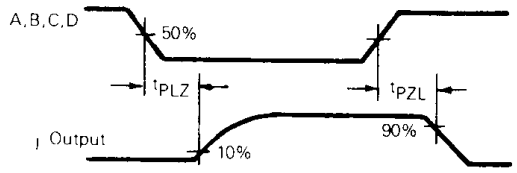


Figure 4

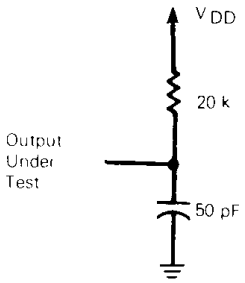
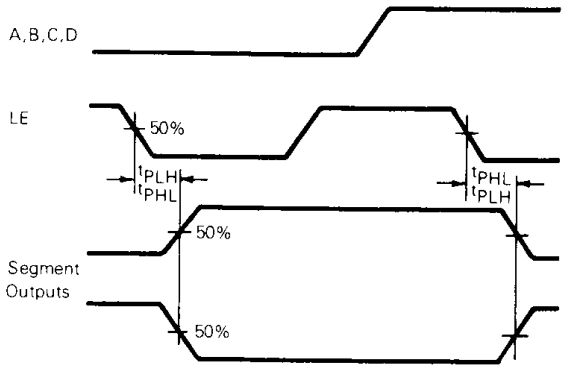


Figure 5



SWITCHING WAVEFORMS

Figure 6

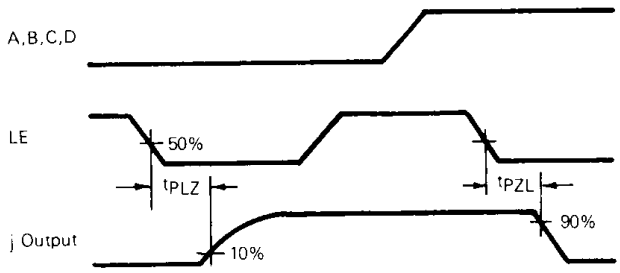
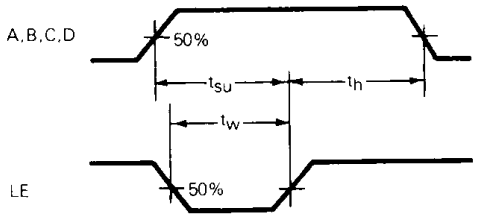


Figure 7



TYPICAL CIRCUIT @ V_{DD} = 5.0 V