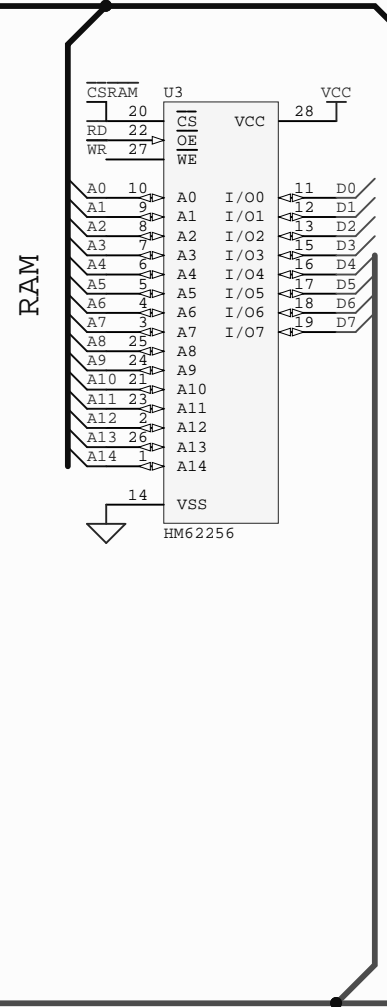
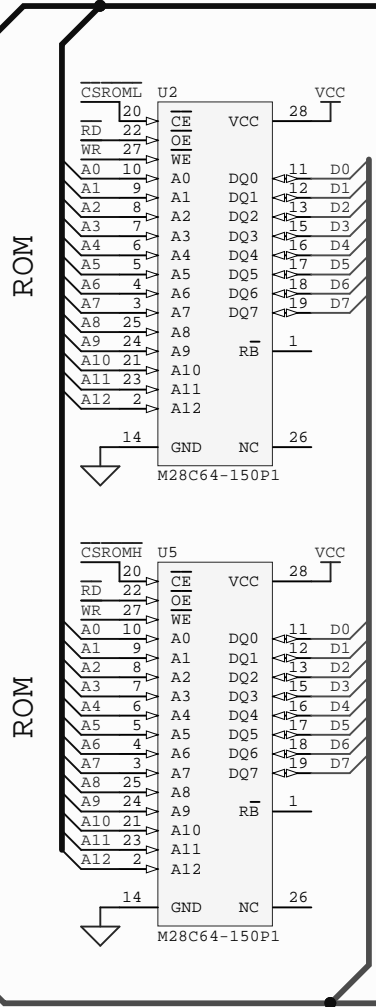
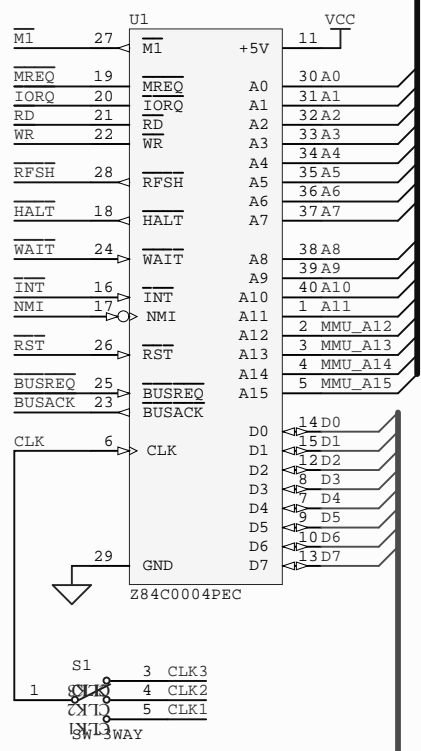
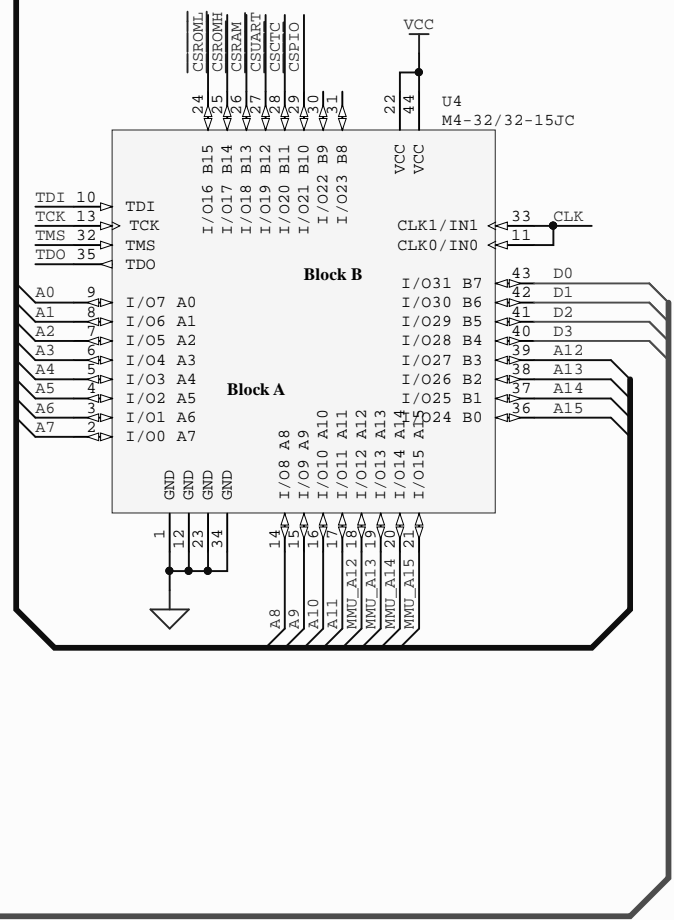


CPU



Address Decoder

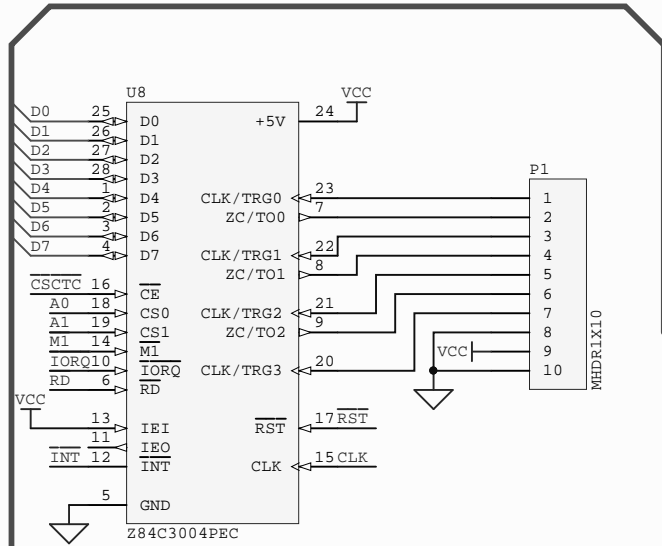


Z80 Micro Computer

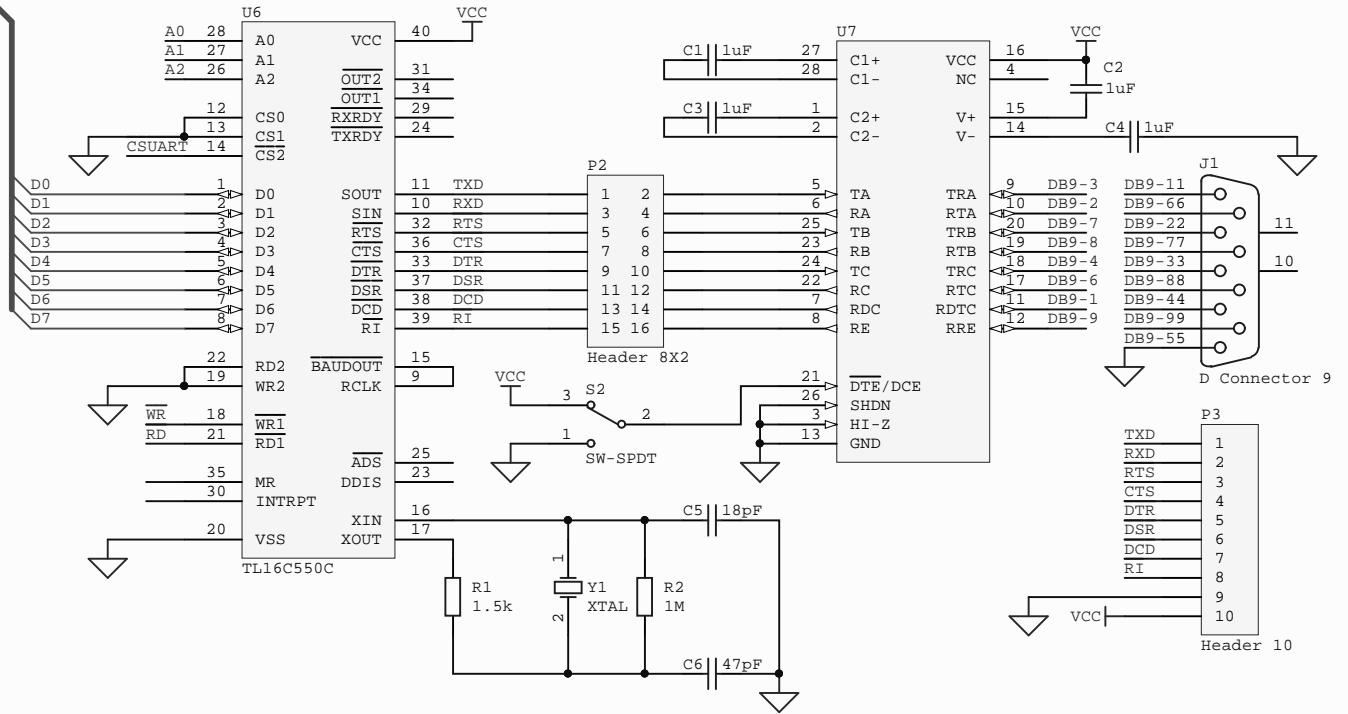
Questo schema e` stato realizzato per il progetto di semestre presso la Scuola delle Arti e Mestieri di Bellinzona. Il progetto di retrocomputing consiste nell'implementazione completa di un architettura tipica per un computer con un processore Z80 dall'hardware al software.

Title z80 Single Board Computer: Base		
Size A4	Number	Revision
Date: 22.05.2017	Sheet 1 of 4	
File: F:\School\...\MainSheet.SchDoc		
Drawn By: Naoki Pross		

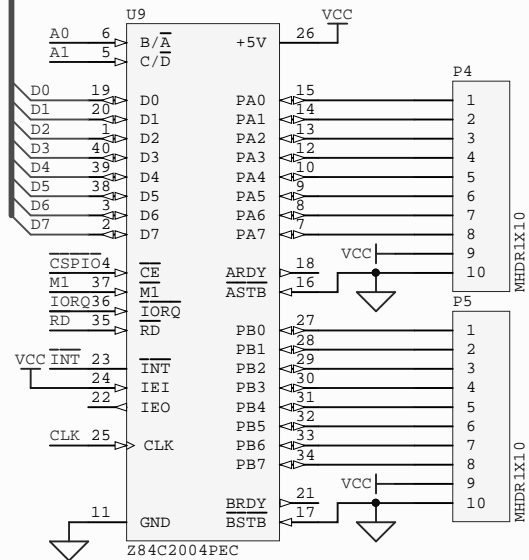
Counter Timer Circuit



Serial Communication Device

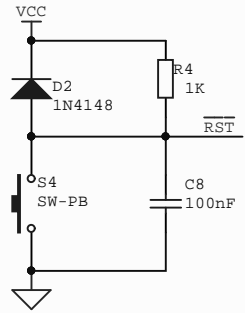


Parallel I/O Controller



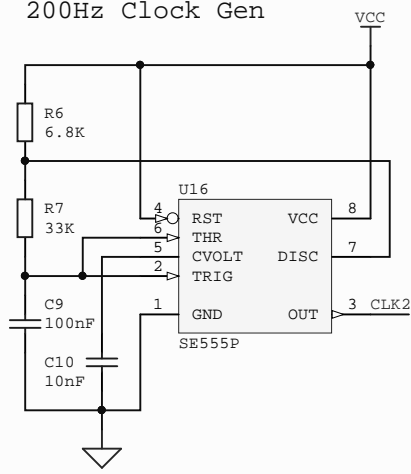
Title z80 Single Board Computer: I/O Devices		
Size A4	Number	Revision
Date: 22.05.2017	Sheet 2 of 4	
File: F:\School\...\IODevices.SchDoc		
Drawn By: Naoki Pross		

Reset Circuit

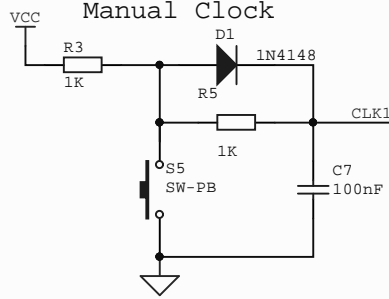


Clock Circuits

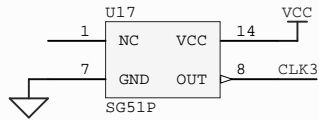
200Hz Clock Gen



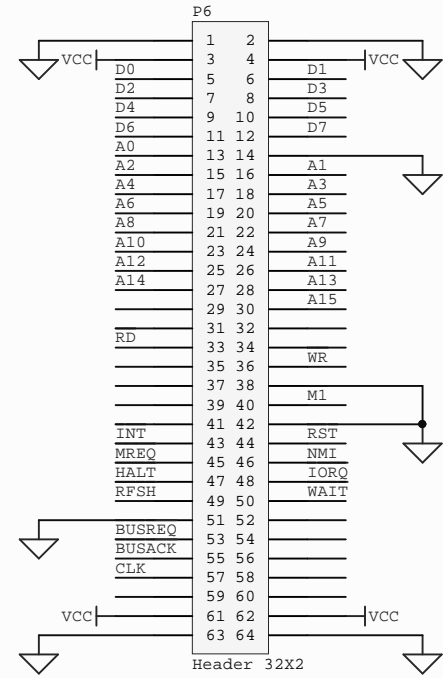
Manual Clock



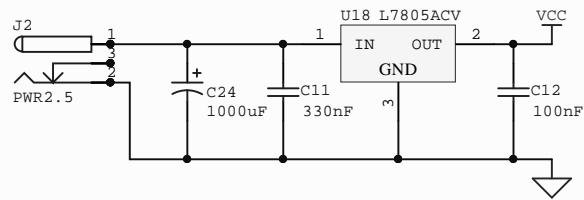
4MHz Clock XTAL



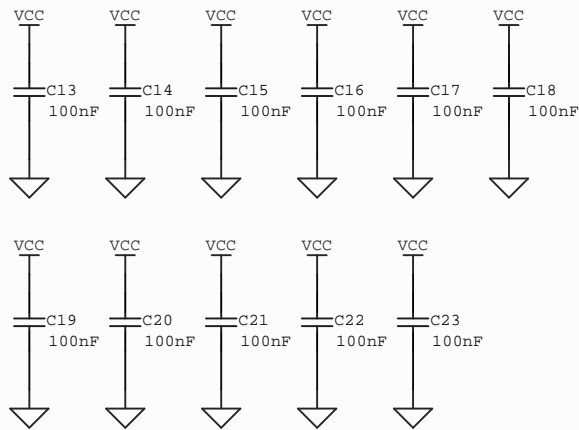
Expansion Connector (DIN41612)



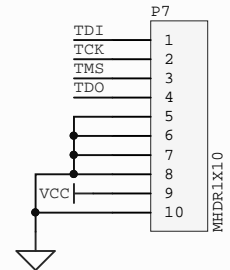
Main Power Supply



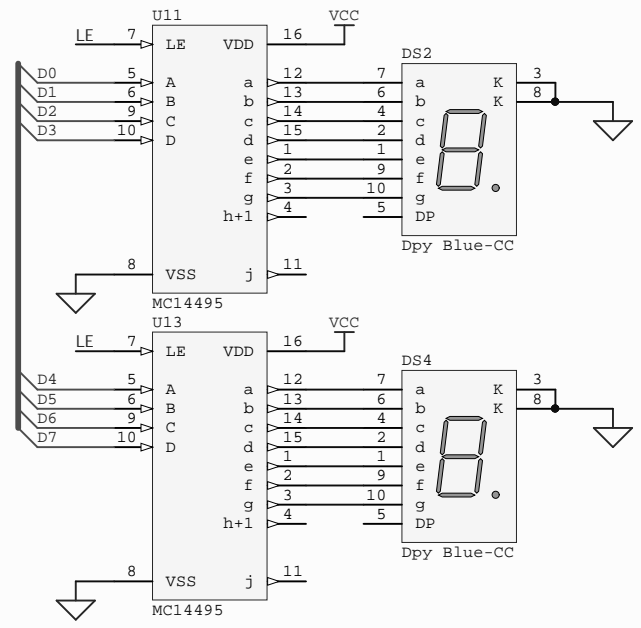
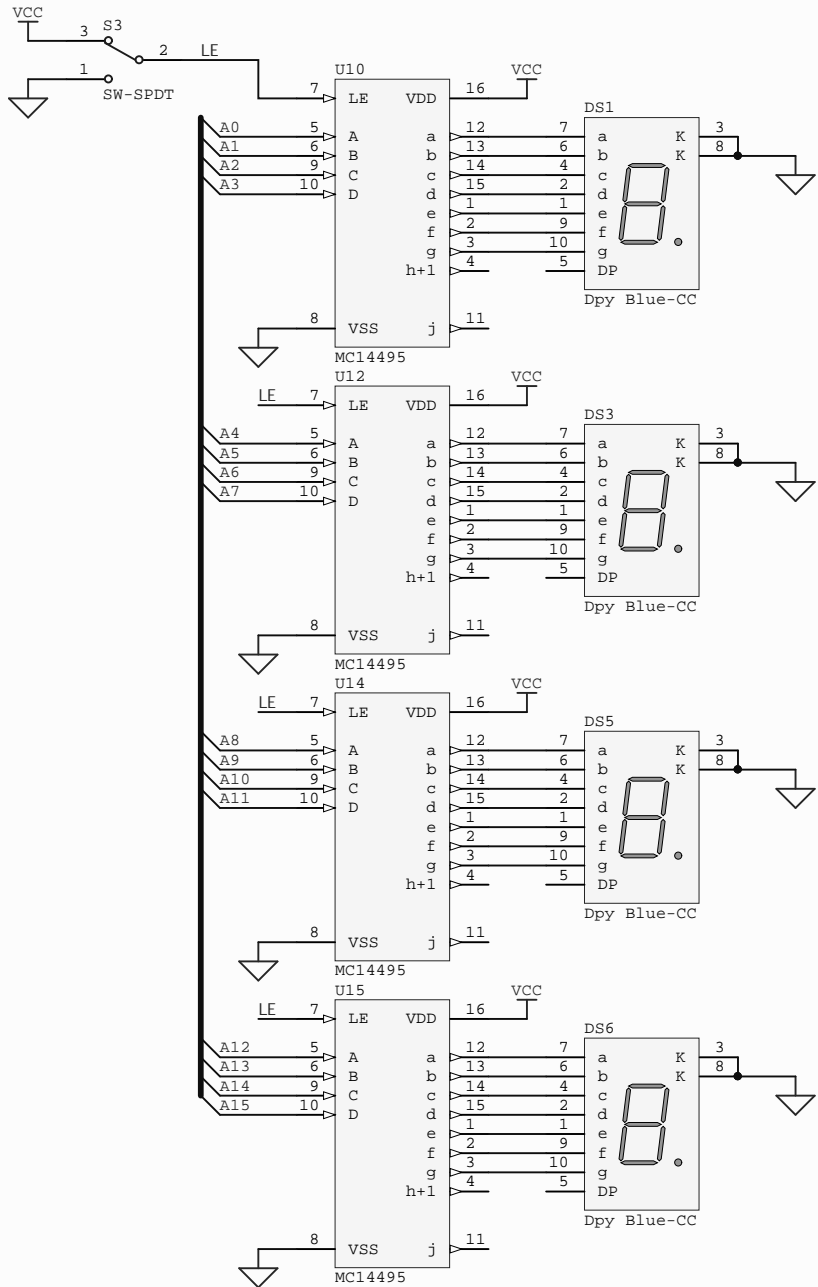
Decoupling Capacitors



Address Decoder CPLD Header



Title z80 Single Board Computer: Peripherals		
Size A4	Number	Revision
Date:	22.05.2017	Sheet 2 of 4
File:	F:\School\...\Peripherals.Sch Drawn By Naoki Pross	



Title z80 Single Board Computer: Bus Data Visualizer		
Size A4	Number	Revision
Date: 22.05.2017	Sheet 4 of 4	
File: F:\School\...\BusViewer.SchDoc Drawn By: Naoki Pross		